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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/989,580	11/20/2001	Gyudong Kim	594728104US	9737

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EXAMINER	
FERRIS, DERRICK W	

ART UNIT	PAPER NUMBER
2663	

DATE MAILED: 06/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/989,580	KIM ET AL.	
	Examiner	Art Unit	
	Derrick W. Ferris	2663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 6-11, and 16-24* is/are rejected.

7)☒ Claim(s) *5 and 12-15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/21/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: please update the incorporated by reference information on page 21.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1-4, 6-11, and 16-24** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,549,971 B1 to *Cecchi et al.* ("*Checchi*") in view of U.S. Patent No. 5,675,584 A to *Jeong et al.* ("*Jeong*").

As to **claim 1**, see e.g., figure 1 of *Checchi*. In particular, a first differential amplifier is shown e.g., as first amplification stage 100 and a second differential amplifier is shown e.g., as second amplification stage 200. As such, a first differential amplifier (i.e., first amplification stage 100 shown in more detail in figure 2) generates a positive polarity data signals VOUT1 and a second differential application circuit generates a negative polarity signals VOUT2. A common mode rejection is independently controlled in each of the first and second differential amplifiers using bias signals generated in response to an output common mode feedback voltage from the first and second differential amplifiers, see e.g., column 5 with respect to feedback node 122 that provides

a negative feedback bias circuit. Finally, an output differential amplifier section that generates an output logic signal VOUT from the positive polarity signals VOUT1 and the negative polarity signals VOUT2, wherein the output logic signal VOUT represents data received on the transmission line, wherein input noise is suppressed using an asymmetric transfer characteristic that offsets output signal logic levels with regard to input noise, see e.g., top of column 7 with respect for compensating for any asymmetries inherent in the amplification stages.

Checchi may be silent or deficient to the further limitation a difference between a positive polarity *transmission line signal* and a positive polarity *transmitter signal* and a difference between a negative polarity *transmission line signal* and a negative polarity *transmitter signal* with respect to a first and second differential amplifier. In particular, *Checchi* discloses a V1 and V2 signal which is differentiated (i.e., a difference between a transmission line signal and a transmitter signal), see e.g., column 3, lines 13-34. However, assuming the above difference is not clear, the examiner also notes the following obviousness rejection as well.

Jeong teaches the further recited limitation above in e.g., figure 1. In particular, *Jeong* teaches a transmission line signal 100 and a transmitter signal 20 with respect to simultaneous transmission, see e.g., column 4, lines 6-32.

The proposed modification of the above-applied reference(s) necessary to arrive at the claimed subject matter would be to modify *Checchi* by clarifying that a transmission signal and transmitter signal are known in the art.

As such, examiner notes that it would have been obvious to one skilled in the art prior to applicant's invention to include the above limitation. In particular, the motivation for modifying the reference or to combine the reference teachings would be to transmit information simultaneously on a transmission line. In particular, *Jeong* cures the above-cited deficiency by providing a motivation found at e.g., column 4, lines 6-32. Second, there would be a reasonable expectation of success since *Checchi* teaches that the invention is applied to a bus topology as shown e.g., in figure 4 with respect to I/O device 414. Thus the references either in singular or in combination teach the above claim limitation(s).

As to **claim 2**, see e.g., the circuitry taught in figure 1 of *Jeong*. Wherein the difference signals are V1 and V2 as taught by *Checchi*.

As to **claim 3**, see e.g., the feedback circuit 122 in figure 2 of *Checchi* for either a first or second differential amplifier.

As to **claim 4**, see e.g., top of column 7 of *Checchi* as previously mention in the rejection for claim 1 with respect to mismatch of the effective channel lengths. In addition, with respect to noise also see e.g., column 3, lines 12-34 of *Checchi*.

As to **claim 6**, see similar rejection to claim 1. As such, *Jeong* teaches the front-end circuit as part of figure 1 where the differential signals are V1 and V2 as taught by *Checchi*.

As to **claim 7**, see similar rejection to claim 1 with respect to the bias circuit as taught e.g., by *Checchi*.

As to **claim 8**, see similar rejection to claim 3.

As to **claim 9**, see similar rejection to claim 3.

As to **claim 10**, see similar rejection to claim 4.

As to **claim 11**, see similar rejection to claim 4.

As to **claim 16**, see similar rejection to claim 1.

As to **claim 17**, see similar rejection to claim 6.

As to **claim 18**, see similar rejection to claim 6.

As to **claim 19**, see similar rejection to claims 1 and 4.

As to **claim 20**, see similar rejection to claim 3.

As to **claim 21**, see similar rejection to claim 1.

As to **claim 22**, see similar rejection to claim 1. The different pairs of signals from the transmission line and the transmitter are e.g., V1 and V2 of *Checchi*.

As to **claim 23**, see similar rejection to claim 1.

As to **claim 24**, see similar rejection to claim 6.

Allowable Subject Matter

4. **Claims 5 and 12-15** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- US006870399B2 with respect to a first and second differential amplifiers 134 and 136 and common feedback circuit, see e.g., bottom of column 7.

- US004598133A with respect to a structure of a differential amplifier that includes common-mode rejection, see e.g., figure 1.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Derrick W. Ferris whose telephone number is (571) 272-3123. The examiner can normally be reached on M-F 9 A.M. - 4:30 P.M. E.S.T.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on (571)272-3139. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Derrick W. Ferris
Examiner
Art Unit 2663

DWF

Derrick W Ferris
5/7/05